REMARKS

This Amendment, submitted in response to the Office Action dated April 5, 2001, is believed to be fully responsive to each point of rejection raised therein. Accordingly, favorable reconsideration on the merits is respectfully requested.

Claims 2-6 and 8-27 remain pending in the application. Claims 17-26 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 2-4, 8-10, 12 and 15 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Nakai et al. (U.S.P. 6,072,454, hereafter "Nakai"). Claims 5-6, 11, 13-14 and 16-27 have been rejected under 35 U.S.C. § 103 as being unpatentable over Nakai in view of Okumura et al. (U.S.P. 6,115,018, hereafter "Okumura"). Applicant amends claims 17-26 to obviate the rejection under Section 112, second paragraph. These amendments do not affect the scope of the claims. Applicant further respectfully submits the following comments in traversal of the art rejections.

As an initial matter, Applicant reserves the right to antedate any art of record should this become necessary at any time.

Applicant's invention relates to a two-dimensional type light modulation device. Detailed descriptions of a preferred embodiment are set forth in the January 3, 2001 Amendment at pages 9-10. Similarly, Nakai is described in the January 3 Amendment at page 10. Applicant refers the Examiner to these descriptions.

Further to these descriptions, it is emphasized that Applicant's invention provides a matrix display, whereby a drive circuit writes data to ferroelectric gate field-effect transistors in order of a row. Additionally, in the present invention, the drive circuit changes the polarization

states of the ferroelectric gate field-effect transistors by changing a gate. As an additional feature of the invention, a drive circuit of the invention includes a single ferromagnetic gate FET, in which the scanning line in a two-dimensional matrix selectively scans a ferromagnetic gate FET directly, and data can be directly written into the ferromagnetic gate FET from the signal line.

Turning to the newly cited reference, Okumura relates to a display device that allows for improved motion representation. In this connection, Okumura relies on small incremental changes in voltages to emphasize the transitions in pixels when an image changes. In particular, when a selecting TFT switch 14-1 is turned off, the feed-through voltage ΔVg is applied to a pixel electrode through a capacitance Cgs between the gate and the source. Thereafter, a corrective force is applied to storage capacitor Cs. Col. 7 line 66 to col. 8, line 7. The corrective voltage is supplied via a control line 13-1. Col. 8, lines 38-48.

The Examiner maintains that Nakai teaches or suggests each feature of independent claims 2, 4, 8 and 10. However, independent claims 2 and 8 each describe that a drive circuit writes data to a field-effect transistor in order of a row. Nakai focuses primarily on the data holding state and changing state of an individual pixel in a matrix. As previously discussed, Nakai is silent as to matrix-wide changes in the display and lacks any specific discussion on the row-order change effected by the drive circuit. The Examiner cites element 102 and col. 14, lines 29-38 of Nakai as teaching this feature. However, element 102 merely corresponds to a scan line. Its operation over several pixel electrodes is not discussed. The text at col. 14 discusses selection of an individual transistor 101. Selection of a ferroelectric gate transistor is based on data supplied on a line 103. However, there is no requirement that the selection signal

for line 103 be provided on a row-basis. The express teachings of Nakai tend to suggest individual activation of a pixel, rather than row or column wide changes in the matrix. Therefore, claims 2 and 8 are not anticipated by Nakai for at least this reason.

With regard to claims 4 and 10, these claims specify that the drive circuit changes a ferroelectric gate of a field-effect transistor to write data based on input data. The Examiner cites col. 4, lines 56-60; col. 5, lines 28-34; col. 10, lines 59-62; and col. 12, lines 63-67 as teaching these features. However, col. 4 merely describes a hold state with no discussion in change of polarization due to gate activity. Col. 5 describes switching based on selection of a data line, which also does not involve a change in the polarization state of a gate. Col. 10 describes the polarization of a memory element 6, which does not provide any information as to whether a gate of a ferroelectric field-effect transistor is changed. Similarly, col. 12 discusses the use of remnant polarization of a ferroelectric substance to provide gradation control of the display. While polarization may arguably provide a means to introduce a current and voltage characteristic, Applicant submits that the way to affect change in polarization in Applicant's invention differs from that of Nakai. It is suggested at col. 15, lines 60-62 of Nakai that a change in the drain voltage, not a gate characteristic effects a polarization change. By contrast, claim 4 describes change of a gate of the transistor. This feature provides a more simplified structure over that of Nakai. Therefore, claims 4 and 10 are not anticipated by Nakai for at least these reasons.

Claims 3, 9, 12 and 15 are further patentable based on their dependency. With further regard to claims 3 and 9, these claims describe writing data and driving modulation of all pixels in common. However, in view of the selective pixel electrode driving in Nakai, the common

modulation of pixels is not taught by the reference. The Examiner has not indicated where Nakai teaches this aspect of the invention.

With regard to independent claims 5-6, 11 and 27, the Examiner cites the combination of Nakai and Okumura to teach each feature of the invention. The Examiner's rejection is not supported for at least five reasons.

First, as an initial matter, the structure of the present invention would not be easily conceived by one skilled in the art based on Nakai and Okumura. In order to select a ferromagnetic gate FET directly, as in the present invention, thorough knowledge about the ferromagnetic gate FET and the driving method for a two-dimensional matrix is required. Unlike Nakai, the present invention does not require a complementary structure having both an n-type and p-type ferromagnetic FET. Rather only a single ferromagnetic gate FET is required.

Second, Applicant submits that one skilled in the art would not combine the teachings of Nakai and Okumura. Nakai relates to a display with reduced voltage requirements. This is achieved by using a ferroelectric material to hold a charge in a stable manner. Okumura relates to a display to provides fast response when a voltage change occurs to represent motion on the display. Though a ferroelectric material has a storage feature, in certain applications, the use of the ferroelectric material tends to introduce a lag, due to the hysteresis effect of a material (See Fig. 12 of Nakai). Due to this lag, one skilled in the art would not include a ferroelectric gate material into the device of Okumura. Moreover, because Nakai requires two control levels stored to ferroelectric storage devices and complementarily providing these signals to a pixel electrode, one skilled in the art would not include a ferroelectric gate transistor directly to drive

lines 101, 103 in Nakai. Additionally, one skilled in the art would not replace the thin film transistor 101 of Nakai with a ferroelectric gate transistor because of the successive steps of inducing voltage fields that are needed to change the polarization of the material. See Nakai, col. 12, lines 51-59. This additional step for clearing a voltage and applying a voltage to exceed a coercive force Ec would defeat the voltage conservation objects of the primary reference. For all of these reasons, Nakai and Okumura each teach away from their combination with the other. Modifications that would make these references pertinent to the present invention would defeat the purpose of each respective patent. Such modifications are not proper. Therefore, independent claims 5-6, 11 and 27 are patentable for at least this reason.

Third, claims 5 and 11 describe row selection and data input relative to signals applied to gate and drains of a ferroelectric gate field-effect transistor. As discussed above, the Okumura does not include a ferroelectric gate field-effect transistor in the configuration as described by claims 5 and 11. The substitution of a ferroelectric gate into Okumura would eliminate the responsiveness to motion that is the principle object of Okumura. In particular, in order to change the polarization of a ferroelectric material, thereby providing a pixel change, this requires that the electric field applied to the material be reduced to zero to eliminate the previously written data. A second electric field exceeding a coercive force would then be applied to write in new data. Nakai, col. 12, lines 51-57. This two-step rewriting of data would significantly slow down the speed at which a pixel output could be changed to represent motion.

Fourth, the Examiner maintains that it would be obvious to combine Nakai and Okumura simply because both references describe active matrix light modulation devices. This rationale for combining the references is completely unsupported. Rather, the references must suggest the

desirability of the modifications suggested. As discussed above, Nakai and Okumura each have different objects within in the field of matrix displays which render their combination improper.

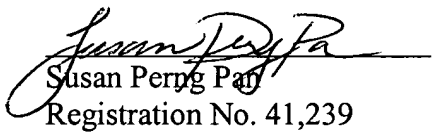
Fifth, Applicant submits that all of the above reasons indicate that the Examiner is merely using impermissible hindsight in making the rejection. Therefore, claims 5-6 and 11 are patentable for at least these reasons, and claims 13-14 and 16-26 are patentable based on their dependency.

With further regard to claims 17-26, these claims describe the use of a single ferroelectric gate transistor. By contrast, Nakai includes a complementary n and p type structure. Moreover, with further regard to claim 27, this claim describes a direct connection of the ferromagnetic gate FET. This feature is not readily apparent from Nakai and Okumura. For example, Nakai requires an intermediate normal FET for pixel selection.

In view of the above, claims 2-6 and 8-27 are in condition for allowance and should be passed to issue at the earliest possible time. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,



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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

17. (Amended) The two-dimensional active-matrix type light-emitting device as set forth in any one of claims 2-6 and 12, wherein the [ferromagnetic FET] ferroelectric gate field-effect transistor comprises a single [ferromagnetic FET] ferroelectric gate field-effect transistor per pixel.

18. (Amended) The two-dimensional active-matrix type light-emitting device as set forth in claim 13, wherein the [ferromagnetic FET] ferroelectric gate field-effect transistor comprises a single [ferromagnetic FET] ferroelectric gate field-effect transistor per pixel.

19. (Amended) The two-dimensional active-matrix type light-emitting device as set forth in claim 14, wherein the [ferromagnetic FET] ferroelectric gate field-effect transistor comprises a single [ferromagnetic FET] ferroelectric gate field-effect transistor per pixel.

20. (Amended) The two-dimensional active-matrix type light-emitting device as set forth in any one of claims 8-11 and 15, wherein the [ferromagnetic FET] ferroelectric gate field-effect transistor comprises a single [ferromagnetic FET] ferroelectric gate field-effect transistor per pixel.

21. (Amended) The two-dimensional active-matrix type light-emitting device as set forth in claim 16, wherein the [ferromagnetic FET] ferroelectric gate field-effect transistor comprises a single [ferromagnetic FET] ferroelectric gate field-effect transistor per pixel.

22. (Amended) The two-dimensional active-matrix type light-emitting device as set forth in any one of claims 2-6 and 12, wherein the [ferromagnetic FET] ferroelectric gate field-effect transistor consists of a single type of semiconductor selected from one of an n-type and a p-type semiconductor.

23. (Amended) The two-dimensional active-matrix type light-emitting device as set forth in claim 13, wherein the [ferromagnetic FET] ferroelectric gate field-effect transistor consists of a single type of semiconductor selected from one of an n-type and a p-type semiconductor.

24. (Amended) The two-dimensional active-matrix type light-emitting device as set forth in claim 14, wherein the [ferromagnetic FET] ferroelectric gate field-effect transistor consists of a single type of semiconductor selected from one of an n-type and a p-type semiconductor.

25. (Amended) The two-dimensional active-matrix type light-emitting device as set forth in any one of claims 8-11 and 15, wherein [ferromagnetic FET] the ferroelectric gate field-effect transistor consists of a single type of semiconductor selected from one of an n-type and a p-type semiconductor.

26. (Amended) The two-dimensional active-matrix type light-emitting device as set forth in claim 16, wherein the [ferromagnetic FET] ferroelectric gate field-effect transistor consists of a single type of semiconductor selected from one of an n-type and a p-type semiconductor.